

**MSX2 PERSONAL COMPUTER SYSTEM
HARDWARE SPECIFICATION**

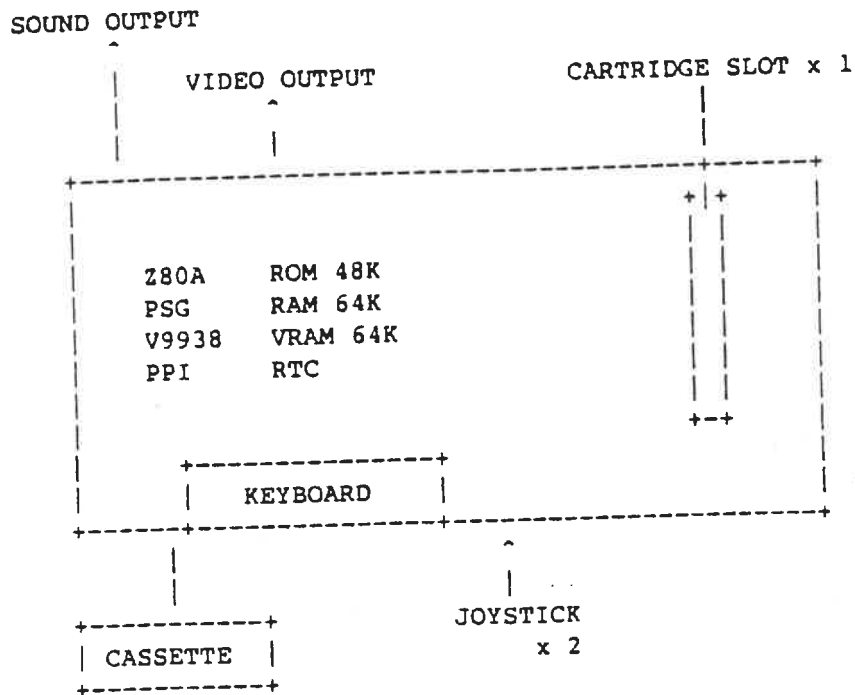
MSX2 Release 5.0 14th Nov. 1985
Revised version of MSX1 Hardware Specification
release 4.1 Feb. 11th, 1985
By Tom Sato MSX Europe
Release 5.2 31st Jan 1986
(C) 1984, 1985 by Microsoft Corp.
(C) 1984, 1985 by ASCII Corp. Microsoft Far East HQ

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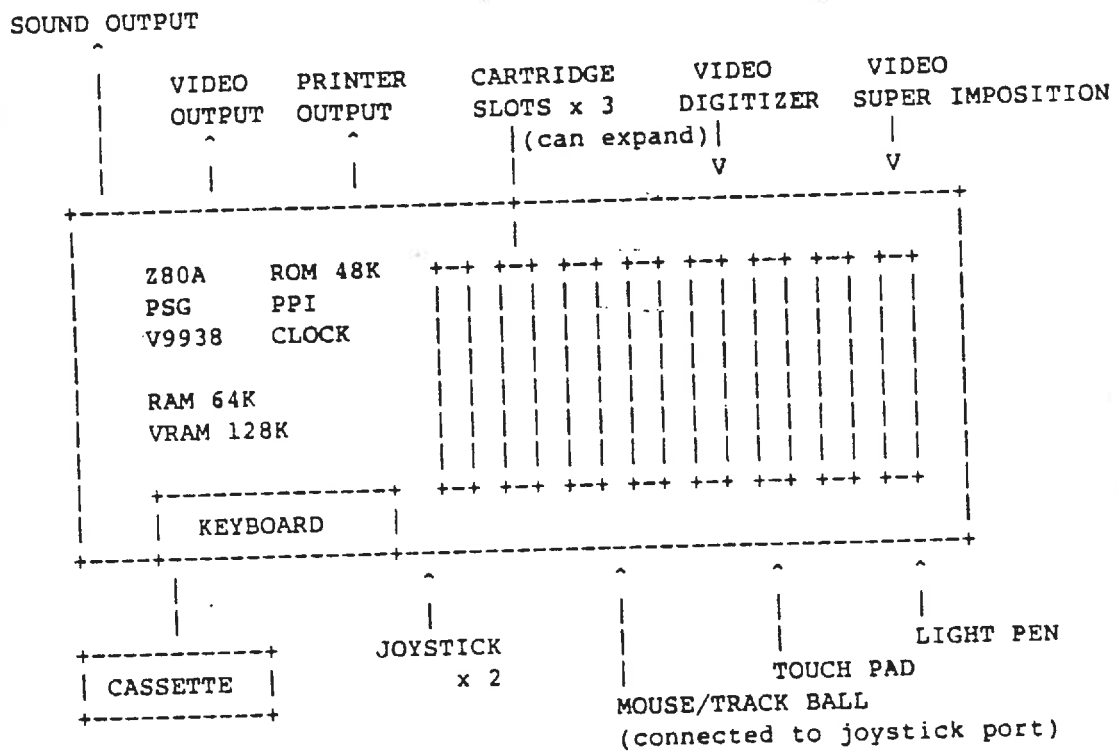
Update history	
March 8th, 1984	Release 3.0
October 22nd, 1984	Release 4.0
February 11th, 1985	Release 4.1
November 14th 1985	Release 5.0
January 10th 1986	Release 5.1
January 31st 1986	Release 5.2

2. SYSTEM CONFIGURATION

2.1 MINIMUM CONFIGURATION



2.2 SYSTEM SOFTWARE SUPPORT LIMIT



3. CPU

Z80A Compatible
CLOCK 3.579545MHz (NTSC Color subcarrier frequency)
1 WAIT in M1 CYCLE

4. MEMORY

4.1 ROM

MSX BASIC Version 2.0 48KB

4.2 RAM

Above 64KB

Using the memory mapper option you can access upto 4MB of RAM.

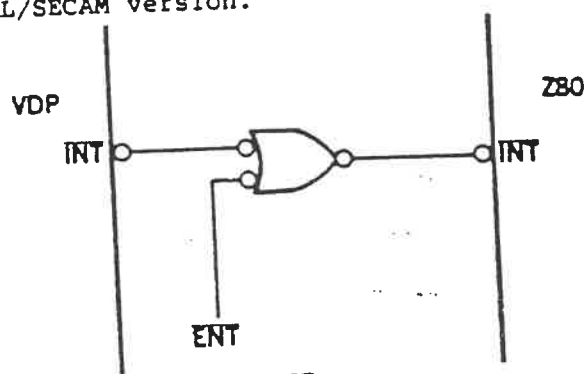
5. INTERRUPT

5.1 NMI

Not used. MSX ROM only provides RAM hook.

5.2 INT

Accept interrupts from VDP and cartridge. The mode of the interrupt is 1. (Branch to 38H) MSX system software uses interrupt from VDP. The interval of the interrupt is 60Hz in NTSC and 50Hz in PAL/SECAM version.



NOTE

It is not possible to support NMI under MSX DOS environment because the address 66H which is entry vector of NMI is occupied by FCB data of DOS.

6. SCREEN DISPLAY

6.1 VDP

YAMAHA V9938 or Compatible

6.2 Character set

Alphanumerical + European + Graphic
256 patterns 8x8 dots

6.3 Sprites

6.3.1 Sprite mode 1

Number of Sprites 32
Number of sprites per horizontal line 4
One colour per sprite
Sprite size 16 x 16 dots Normal size
 16 x 16 dots Double size
 8 x 8 dots Normal size
 8 x 8 dots Double size

6.3.2 Sprite mode 2

Number of Sprites 32
Number of sprites per horizontal line 8
Colour (back/foreground) may be specialised for
each horizontal line
Sprite size 16 x 16 dots Normal size
 16 x 16 dots Double size
 8 x 8 dots Normal size
 8 x 8 dots Double size

6.4 List of display modes

6.4.1 SCREEN 0:WIDTH 40

Pattern size	6 dots (w) x 8 dots (h)
Patterns	256 types
Screen pattern count	40 (w) x 24 (h) patterns
Pattern colours	Two colours out of 512 colors (per screen)
VRAM area per screen	4K bytes

6.4.2 SCREEN 0:WIDTH 80

Pattern size	6 dots (w) x 8 dots (h)
Patterns	256 types
Screen pattern count	80 (w) x 24 (h) patterns
	80 (w) x 26.5 (h) patterns
Pattern colours	Two colours out of 512 colors (per screen)
	four if using blinking
VRAM area per screen	8K bytes

6.4.3 SCREEN 2

Screen composition	64 (w) x 48 (h) colour blocks
Colour blocks	Sixteen colours out of 512 colours
Sprite mode	Sprite mode 1
VRAM area per screen	4K bytes

6.4.4 SCREEN 1

Pattern size	8 dots (w) x 8 dots (h)
Patterns	256 types
Screen pattern count	32 (w) x 24 (h) patterns
Pattern colours	16 colours out of 512
Sprite mode	Sprite mode 1
VRAM area per screen	4K bytes

6.4.5 SCREEN 3

Pattern size	8 dots (w) x 8 dots (h)
Patterns	768 types
Screen pattern count	32 (w) x 24 (h) patterns
Pattern colours	16 colours out of 512 per screen
VRAM area per screen	16K bytes
Sprite Mode	Sprite mode 1

6.4.6 SCREEN 4

Pattern size	8 dots (w) x 8 dots (h)
Patterns	768 types
Screen pattern count	32 (w) x 24 (h) patterns
Pattern colours	16 colours out of 512 per screen
VRAM area per screen	16K bytes
Sprite Mode	Sprite mode 2

6.4.7 SCREEN 5

Bit-mapped Graphics Mode

Screen size	256 (w) x 212 (h) dots
	256 (w) x 192 (h) dots
Screen colours	16 colors out of 512
VRAM area per screen	32K bytes
Sprite mode	Sprite Mode 2

6.4.8 SCREEN 6

Bit-mapped Graphics Mode

Screen size	512 (w) x 212 (h) dots
	512 (w) x 192 (h) dots
Screen colours	4 colors out of 512
VRAM area per screen	64K bytes
Sprite mode	Sprite mode 2

Requires 128K of VRAM

6.4.9 SCREEN 7

Bit-mapped Graphics Mode

Screen size	512 (w) x 212 (h) dots
	512 9w) x 192 9h) dots
Screen colours	16 colors out of 512
VRAM area per screen	64K bytes
Sprite Mode	Sprite mode 2

Requires 128K of VRAM

6.4.10 SCREEN 8

Bit-mapped Graphics Mode

Screen size	256 (w) x 212 (h) dots
	256 (w) x 192 9h) dots
Screen colours	256 colours per screen
VRAM area per screen	64K bytes
Sprite Mode	Sprite mode 2

Requires 128K of VRAM

7. KEYBOARD

7.1 Layout

- 0. Japan
- 1. International (USA)
- 2. UK
- 3. France
- 4. Germany
- 5. Italy
- 6. Spain
- 7. Arabia
- 8. Korea
- 9. Russian
- 10. Denmark
- 11. Sweden
- 12. Finland

See Appendix for Keyboard layouts

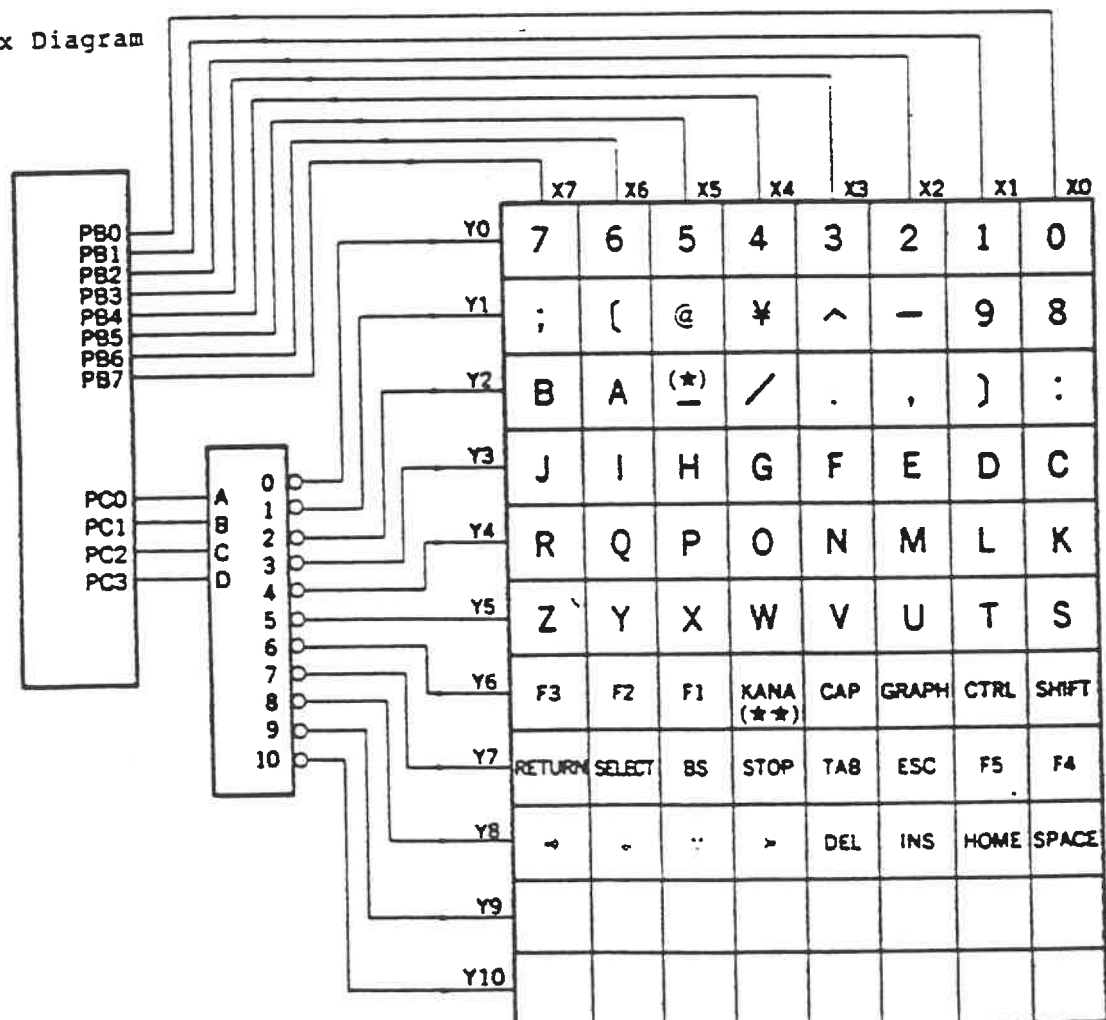
7.2 Scanning

Software scanning driven by VDP interrupt

7.3 Number of Keys

72

7.4 Matrix Diagram



★ Underscore character.

★★ Code Lock key in international versions.

8. SOUND

8.1 LSI

GI AY-3-8910 Compatible

8.2 OCTAVE

8 Octaves (3 Voices output)

8.3 SOUND EFFECT

Yes

8.4 SOFTWARE SOUND OUTPUT

1 bit from output port

8.5 OUTPUT LEVEL

-5dbm (If the system has output connector)

8.6 CONNECTOR

RCA 1 pins

or RGB connector with audio output

8.7 OPTION

MSX AUDIO

Please see MSX Audio specification

9. CASSETTE INTERFACE

9.1 INPUT

From the microphone terminal of tape recorder

9.2 OUTPUT

To the earphone terminal of tape recorder

9.3 SYNCHRONIZATION

Asynchronous by the software

9.4 BAUD RATE

1200 Baud(1200Hz - 1 wave "0", 2400Hz - 2 waves
"1") (Default)

2400 Baud(2400Hz - 1 wave "0", 4800Hz - 2 waves
"1") (Change by software)
(Tape recorder may have to be specified by the
manufacturer when used under 2400 Baud mode)

9.5 MODULATION

FSK (Frequency Shift Keying) by the software

9.6 DEMODULATION

By the software. The system software automatically
detects the baud rate when receiving the data.

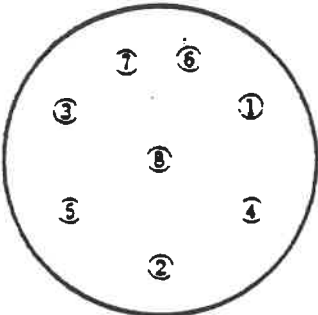
9.7 MOTOR CONTROL

Yes

9.8 CONNECTOR

DIN 45326 (8 pins)

9.9 TABLE OF SIGNAL PINS

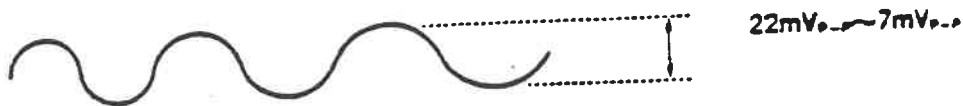
PIN No.	SIGNAL NAME	DIRECTION	PIN CONNECTION
1	GND	---	
2	GND	---	
3	GND	---	
4	CMTOUT	OUTPUT	
5	CMTIN	INPUT	
6	REMOTE +	OUTPUT	
7	REMOTE -	OUTPUT	
8	GND	---	

9.10 SAVE Level

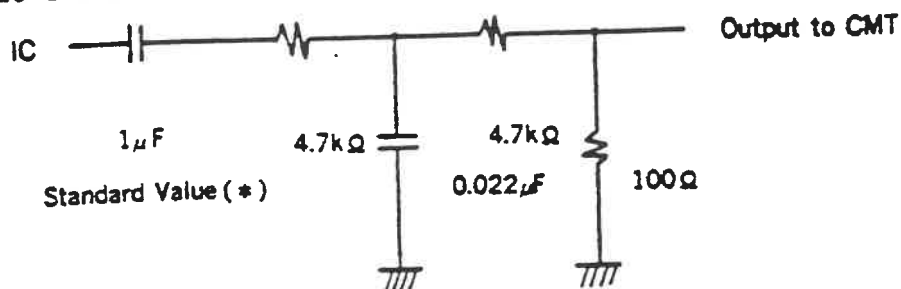
The constants in the SAVE circuit should be adjusted so as to perform the output level as follows:-

Output level $-45 \text{ dBm} \pm 5 \text{ dBm}$ ($0 \text{ dBm} = 0.775 \text{ V}$)

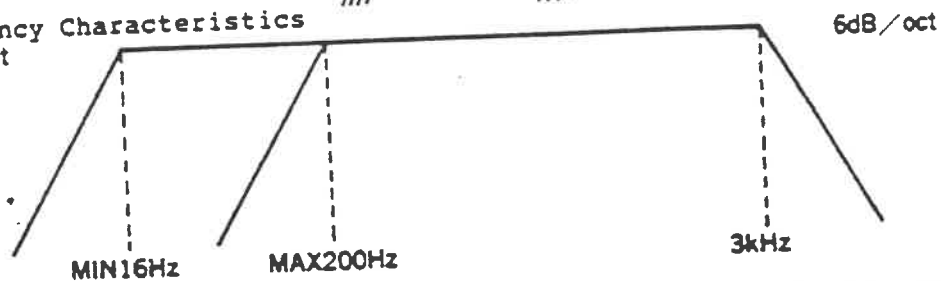
The output should be $22 \text{ mVp-p} \sim 7 \text{ mVp-p}$ at 1200 Hz input signal.



9.11 Sample Circuit for SAVE



9.12 Frequency Characteristics



Lower Cutoff Frequency (*)

Higher Cutoff Frequency

- * Note that the lower cutoff capacitor is to protect the IC of MSX. cassette tape recorders themselves will not be harmed even if it is not there. The capacitance may be in the range $0.1 \sim 2.2 \mu\text{F}$. Adjust the capacitor to limit the lower cutoff frequency in the range $16 \sim 200 \text{ Hz}$, if the output impedance of IC is too high.

10. JOYSTICK INPUT/OUTPUT PORT (2 PORTS)

10.1 LSI

AY-3-8910 compatible

10.2 I/O

Input 4 bit, output 1 bit, bidirectional 2 bits per each port

10.3 LOGIC

Active high

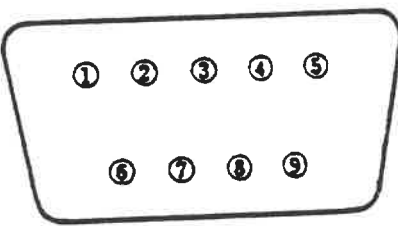
10.4 LEVEL

TTL

10.5 CONNECTOR

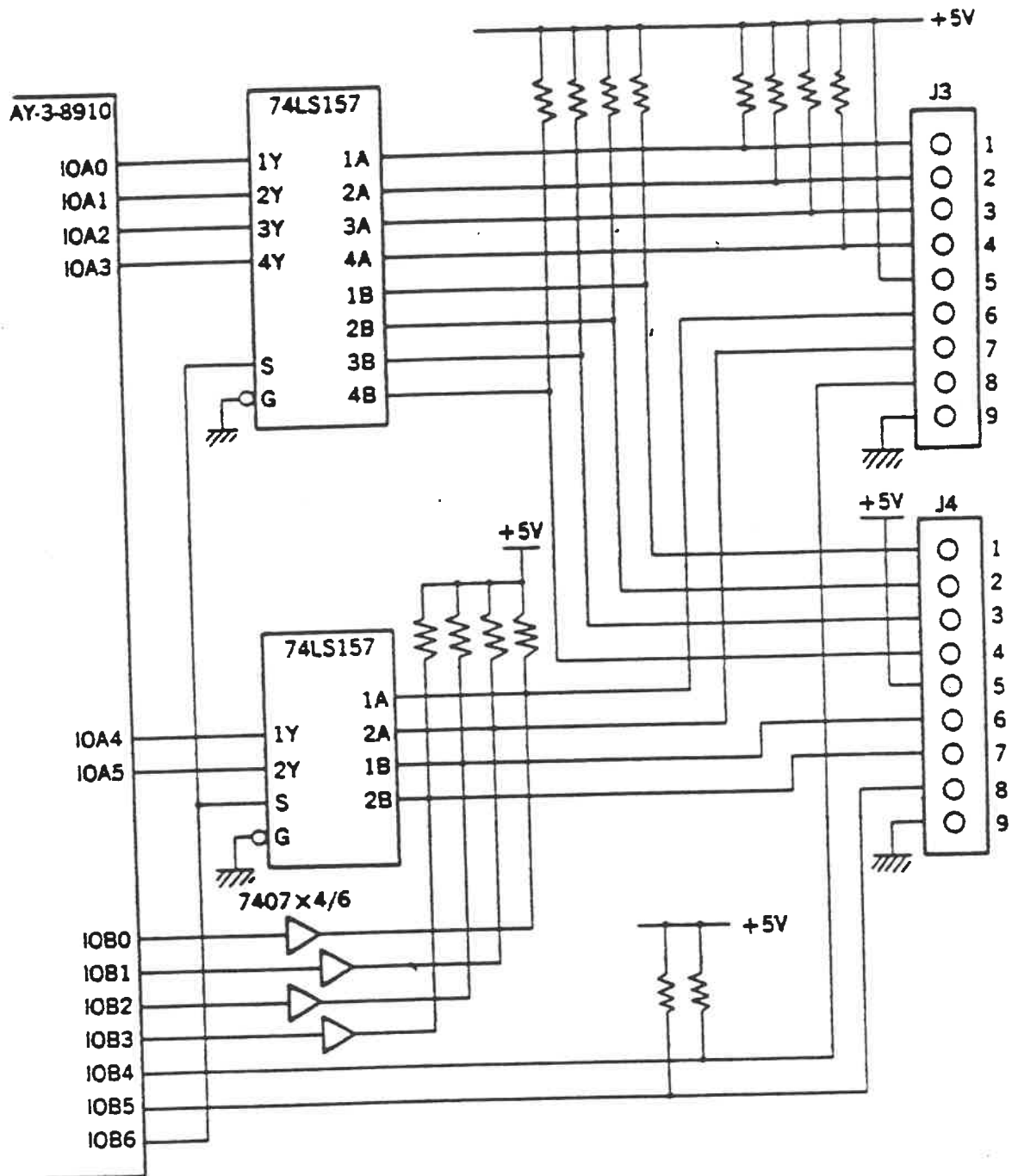
AMP 9 pins compatible

10.6 LIST OF PINS

PIN No.	SIGNAL NAME	DIRECTION	PIN CONNECTION
1	FWD	INPUT	
2	BACK	INPUT	
3	LEFT	INPUT	
4	RIGHT	INPUT	
5	+ 5V	---	
6	TRG 1	INPUT/ OUTPUT	
7	TRG 2	INPUT/ OUTPUT	
8	OUTPUT	OUTPUT	
9	GND	---	

* Current capacity is 50mA each

Circuit Diagram



All registers are 10k ohm typically.

11. PRINTER INTERFACE

11.1 SPECIFICATION

8 bit parallel. Handshakes by BUSY and STROBE signal

11.2 LEVEL

TTL

11.3 CHARACTER CODE

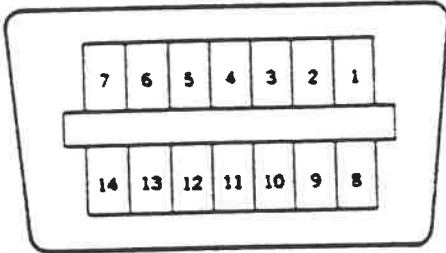
Same as MSX display mode.

11.4 CONNECTOR

AMP 14 pins compatible

11.5 LIST OF PINS

(Signals with overscoring are negative logic)

PIN NO.	SIGNAL NAME	PIN CONNECTION
1	PSTB	
2	PDB0	
3	PDB1	
4	PDB2	
5	PDB3	
6	PDB4	
7	PDB5	
8	PDB6	
9	PDB7	
10	N.C.	
11	BUSY	
12	N.C.	
13	N.C.	
14	GND	

12. FLOPPY DISK INTERFACE

12.1 Contains 16K bytes of ROM at 4000H that includes:

- * MSX DOS KERNEL
- * MSX DISK BASIC
- * PHYSICAL DISK I/O DRIVER
(Supplied by each manufacturer)

The hardware interface is not specified. The physical disk I/O driver supplied by manufacturer should virtualize the hardware difference.

Floppy format is MS-DOS compatible

Appllication software should use the BDOS call to control the disk drive

13. CARTRIDGE SLOT

o CONCEPT OF SLOT

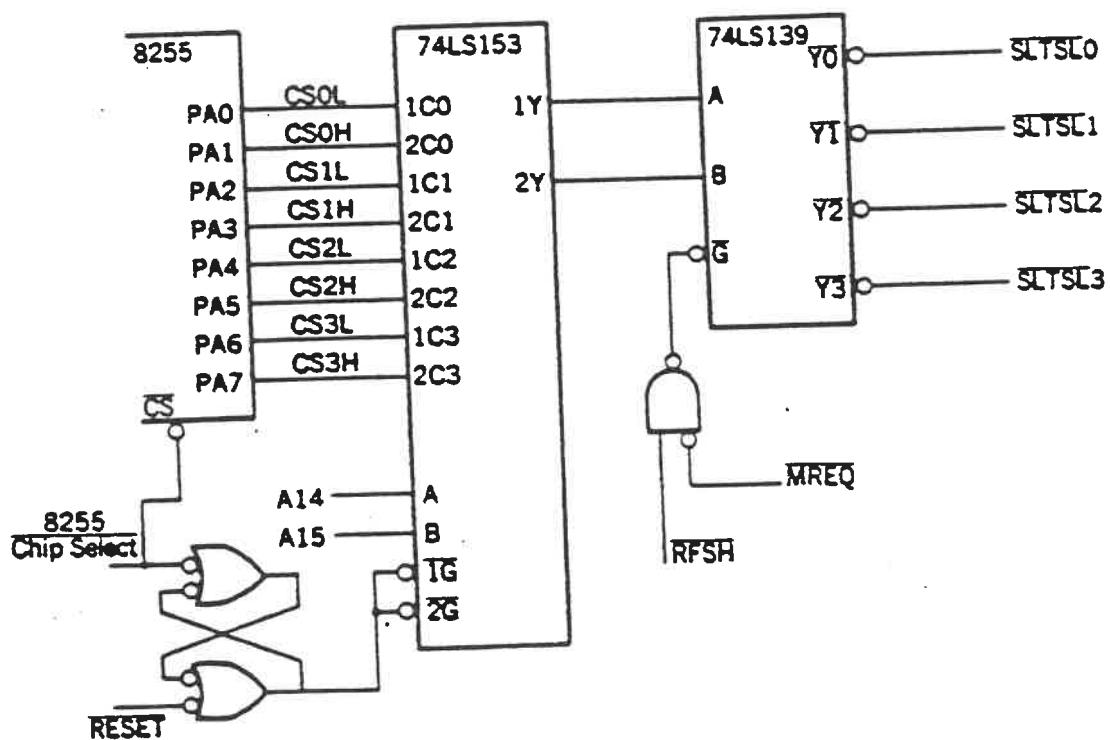
For a structure of 64 KB memory space, the concept of slot and memory bank is nearly the same. But the CPU can choose the cartridge by the slot number in which it is inserted.

The slot concept is originated from the standpoint of the software, and so, the software is independent to the number of the slot that has actual slot opening.

o ADVANTAGES OF SLOT STRUCTURE

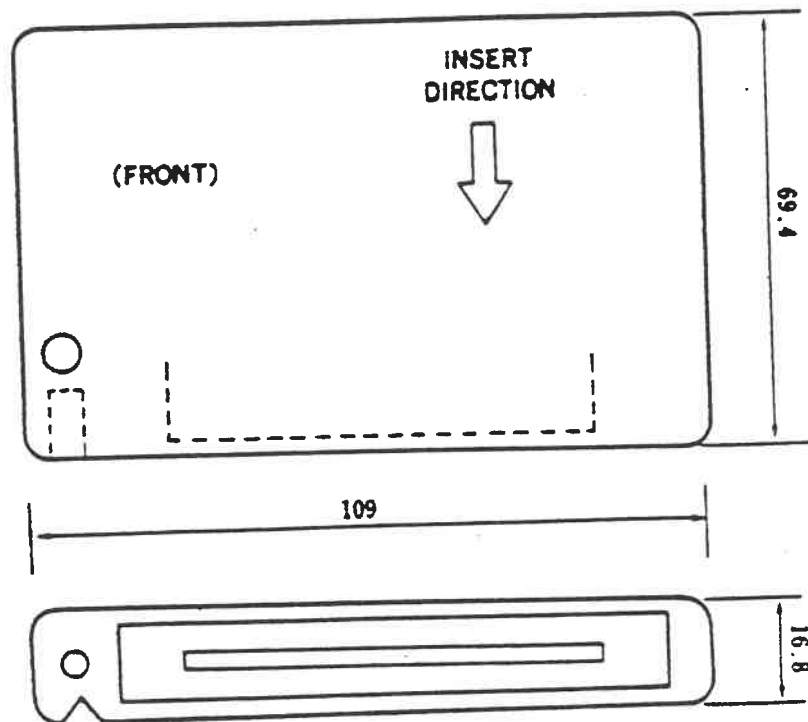
In the common bus structure, when the memory bank number is even, the device select signal connected to the bus cannot distinguish different devices if they use the same memory area. In this case, not only the system becomes out of disorderly, but hardware will suffer also. By using slot select signal to choose each of the devices, there will be no such problem. Program dealing with two or more devices at the same memory area is possible. This is favorable to the flexibility and expandability of the system.

o Circuit Diagram

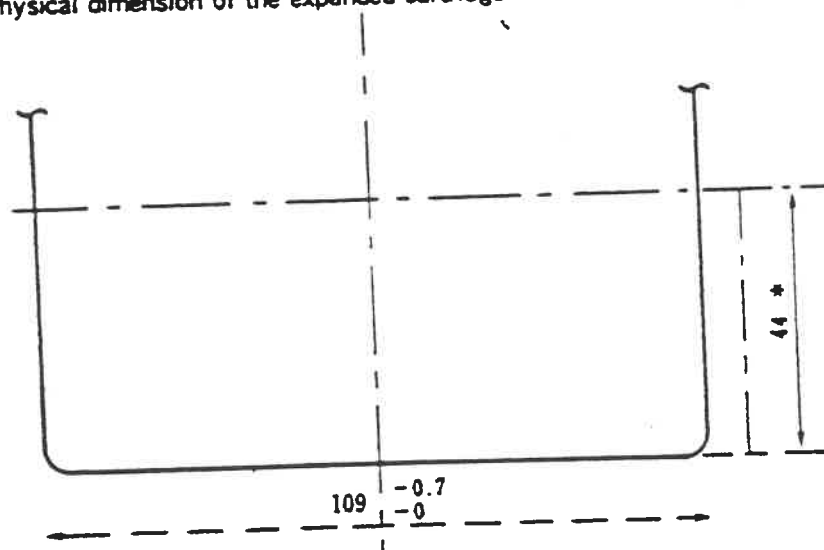


13.1 PHYSICAL SPECIFICATION OF THE CARTRIDGE

o Physical dimension of the standard cartridge



o Physical dimension of the expanded cartridge



13.2 CARTRIDGE BUS

LIST OF SIGNAL PINS

(Overscored signals are negative logic)

PIN NO.	NAME	* I/O	PIN NO.	NAME	* I/O
1	$\overline{\text{CS1}}$	O	2	$\overline{\text{CS2}}$	O
3	$\overline{\text{CS12}}$	O	4	$\overline{\text{SLTSL}}$	O
5	RESERVED #	-	6	$\overline{\text{RFSH}}$	O
7	$\overline{\text{WAIT}}\%$	I	8	$\overline{\text{INT}}\%$	I
9	$\overline{\text{M1}}$	O	10	$\overline{\text{BUSDIR}}$	I
11	$\overline{\text{IORQ}}$	O	12	$\overline{\text{MERQ}}$	O
13	$\overline{\text{WR}}$	O	14	$\overline{\text{RD}}$	O
15	$\overline{\text{RESET}}$	O	16	RESERVED #	-
17	A9	O	18	A15	O
19	A11	O	20	A10	O
21	A7	O	22	A6	O
23	A12	O	24	A8	O
25	A14	O	26	A13	O
27	A1	O	28	A0	O
29	A3	O	30	A2	O
31	A5	O	32	A4	O
33	D1	I/O	34	D0	I/O
35	D3	I/O	36	D2	I/O
37	D5	I/O	38	D4	I/O
39	D7	I/O	40	D6	I/O
41	GND	-	42	CLOCK	O
43	GND	-	44	SW1	-
45	+5V	-	46	SW2	-
47	+5V	-	48	+12V	-
49	SOUNDIN	I	50	-12V	-

* The direction of input/output is based on basic unit side.

Reserved PIN must not be used. (no connection)

% OPEN COLLECTOR Output

13.3 SIGNAL PIN ILLUSTRATION

(Overscored signals are negative logic)

PIN NO.	NAME	DESCRIPTION
1	$\overline{\text{CS1}}$	ROM 4000~7FFF selected signal
2	$\overline{\text{CS2}}$	ROM 8000~BFFF selected signal
3	$\overline{\text{CS12}}$	ROM 4000~BFFF selected signal (for 256K ROM)
4	$\overline{\text{SLTSL}}$	Slot select signal
5	RESERVED	For future use only. Do not use this pin.
6	$\overline{\text{RFSH}}$	Refresh signal
7	$\overline{\text{WAIT}}$	Wait signal to CPU
8	$\overline{\text{INT}}$	Interrupt request signal
9	$\overline{\text{M1}}$	Fetch cycle signal of CPU
10	$\overline{\text{BUSDIR}}$	This signal controls the direction of external data bus buffer when the cartridge is selected. It is low level when the data is sent by the cartridge.
11	$\overline{\text{IORQ}}$	I/O request signal
12	$\overline{\text{MERQ}}$	Memory request signal
13	$\overline{\text{WR}}$	Write signal
14	$\overline{\text{RD}}$	Read signal
15	$\overline{\text{RESET}}$	System reset signal
16	RESERVED	For future use only. Do not use this pin.
17~32	A0~A15	Address bus
33~40	D0~D7	Data bus
41	GND	Ground
42	CLOCK	CPU clock 3.579MHz
43	GND	Ground
44, 46	SW1, SW2	Insert/ remove detect for protection
45, 47	+5V	+5V power supply
48	+12V	+12V power supply
49	SOUNDIN	Sound input (-5dbm)
50	-12V	-12V power supply

NOTE

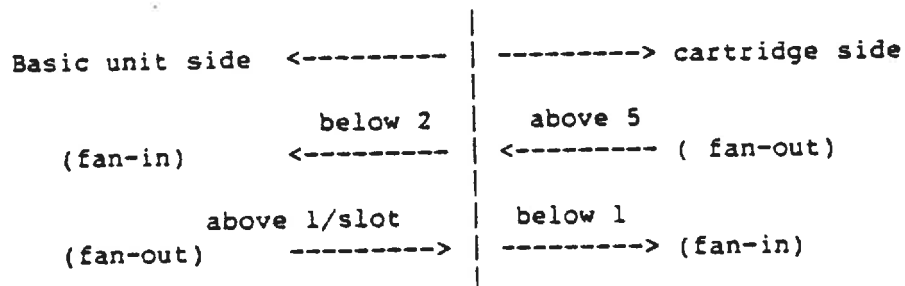
SW1 and SW2 are connected inside the cartridge.

CS signals imply memory request and read signal. Therefore they cannot be used as chip select for writable devices such as RAMs.

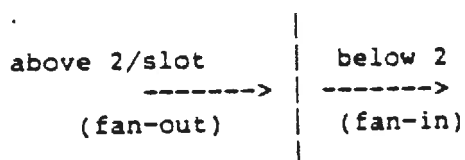
13.4 CONDITION OF CARTRIDGE CONNECTION

o Fan-in, fan-out (LS-TTL load)

Data and Address bus



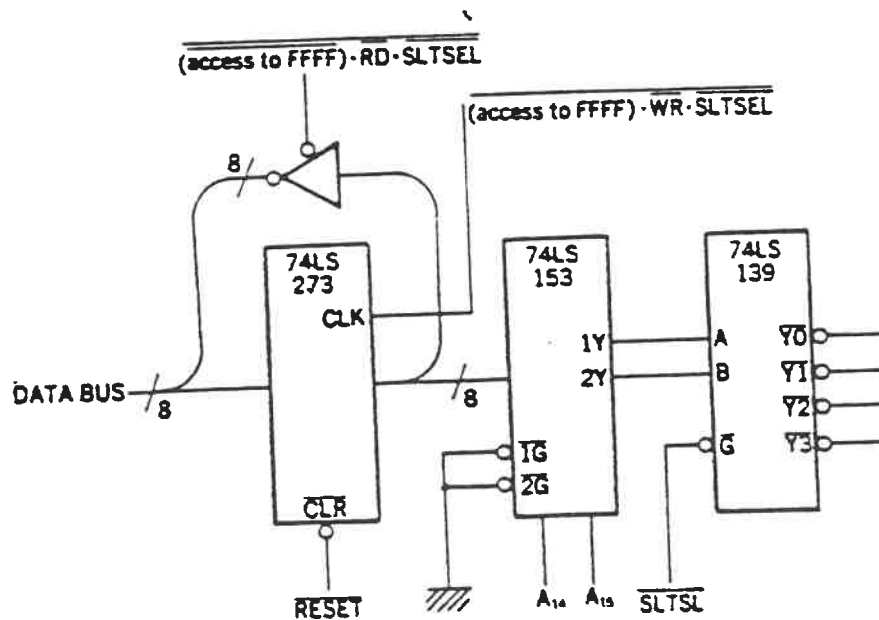
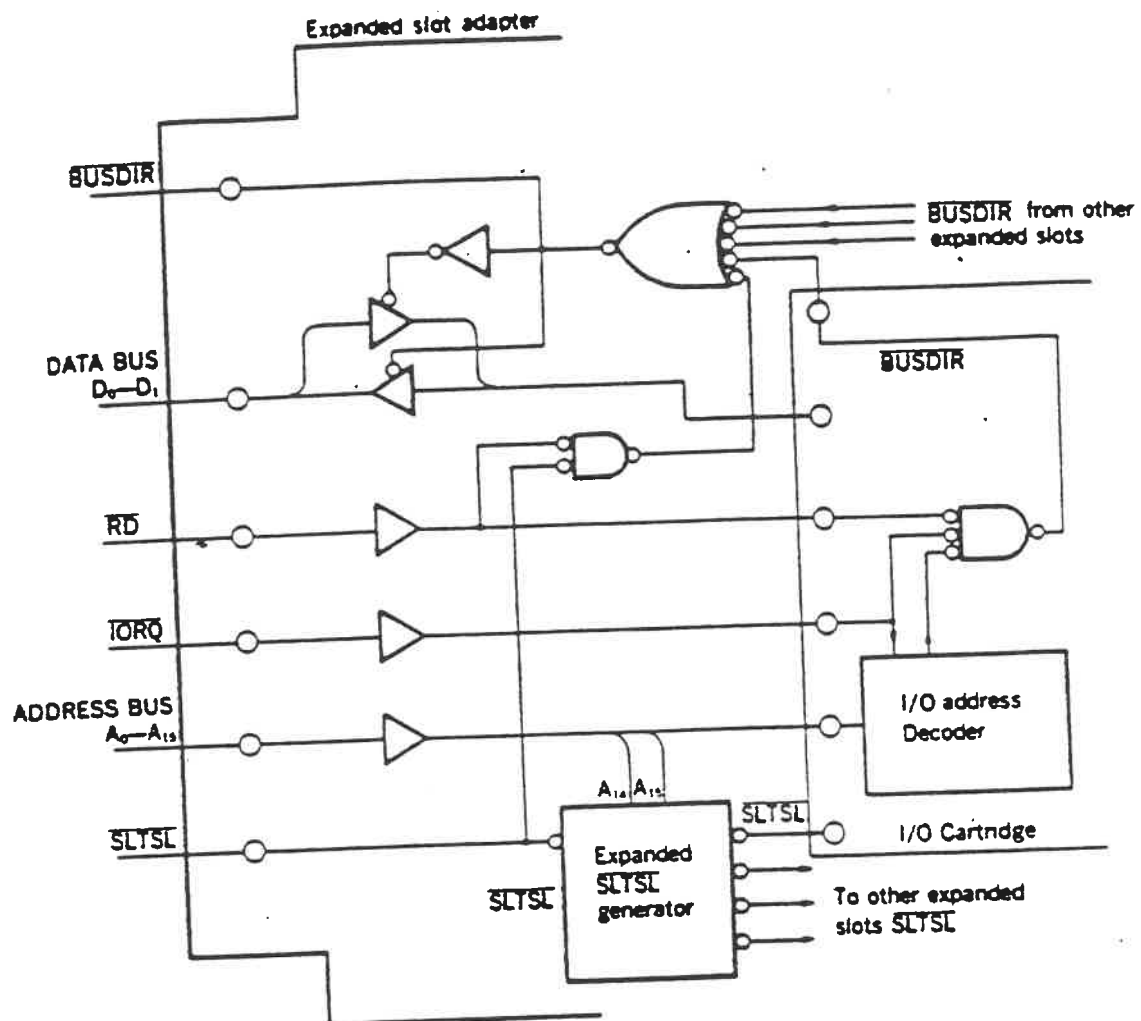
o control signals

o Voltage level
TTL level

13.5 POWER CAPACITY

+5V	300mA/slot
+12V	50mA/system
-12V	50mA/system

13.6 Sample Circuit Diagram of Expanded Slot Select Signal



13.7 Notes on Slot Expansion

- o To expand slots, the additional slots are expanded from primary slots. Primary slots are those slots which are managed by the basic slot select register placed in port A of 8255. Therefore, to select the expanded slot, first select the primary slot to which the expanded slot is connected, and select the desired expanded slot.
- o Those slots which are attached on the MSX computer itself have to be primary slots. Because there are significant differences between primary slots and secondary slots, there should be a clear indication to tell which kind of slot are used in an expansion adapter.
- o The location of the slot select register for the expanded slots is memory address FFFF of the primary slot. To make it possible to differentiate the register from the ordinary RAM, complement the output of the register. That is, when the register is read the read data is the complement of the actual value of the register.
- o A maximum of four cartridges can be connected to the cartridge bus. Therefore buffers are necessary to put more than five slots onto the system. The control signal that controls the direction of these buffers is BUSDIR. Those devices that send signals to CPU and are placed in an expanded slot have to send BUSDIR signals as well to change the direction of the buffer from expanded slots to CPU. However, for the access to memory, it is possible to know the direction of the bus by using the slot select signal to the primary slot, memory request signal and read/write signal. So the direction of the buffer should be controlled around the buffer circuitry. Those cartridges which contain only ROM/RAM will be cheaper because they do not have to manage BUSDIR signal, but those cartridges that contain some devices which send signals to the CPU (devices that respond to INP instruction or devices that are responsible for supplying the address in response to mode 2 of interrupt) must force BUSDIR at 'L' level when they send data to CPU.

NOTES ON SYSTEM EXPANSION

13.8 Notes on I/O Expansion

- o In Z-80 based systems, it is common to place I/O devices in I/O address space. But the MSX system is designed to be flexible and expandable, it is possible to add some I/O devices cartridges using that share the same address space. If this is the case, none of those devices can be accessed properly.

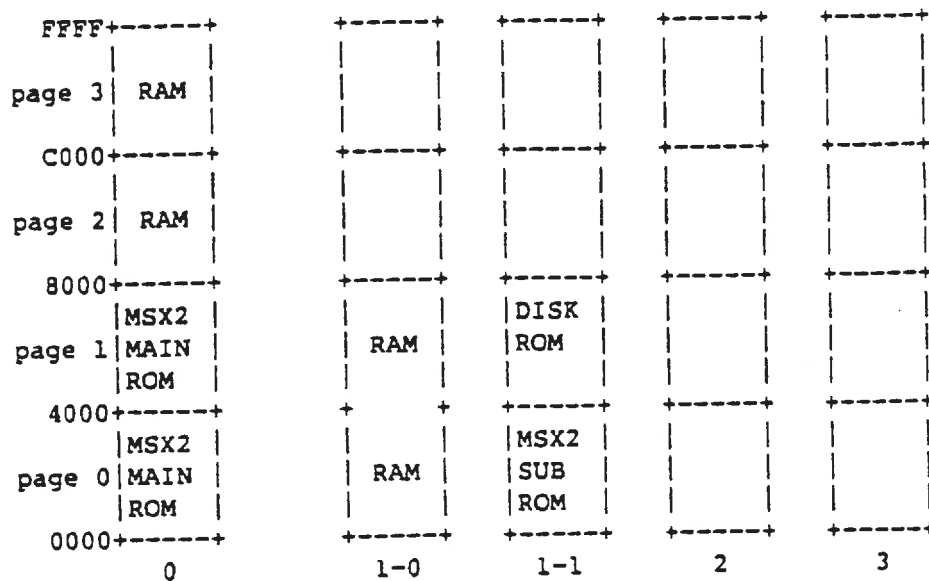
To avoid this situation, it is preferred to place I/O devices in the memory spaces because they are managed by slot select logic and no memory can be accessed simultaneously when they are placed in different slots. But devices that are placed in memory space can not be accessed by software that runs in different slots. So those devices that are general to any software such as VDP have to be placed in I/O address space. In some cases, it is cheaper to use I/O address space because only 8 bit address information will should be decoded.

We defined I/O address space from 40 to FF for system devices. But the addresses below 3F are left free. Anyone can use this address space, but nobody can tell can tell you if somebody else uses the same address that you are using. So recommend to use the memory address spaces rather than I/O addresses space. We will assign the reserved addresses which are to those MSX standard devices.

14. MEMORY MAP

o Following is an example of the memory map.

EXAMPLE



- o MSX BASIC uses the largest available RAM area that is installed from FFFF to 8000 contiguous for its system working RAM area. This can be placed on any slots including expanded slots.
- o Slot select register, which is at port A of 8255, maps physical memory space to the logical CPU memory space in 16K byte units (page). For example, the following value in slot select register allocates page 0 and 1 from slot 0, page 2 from slot 2 and page 3 from slot 0.

MSB - 7 6 5 4 3 2 1 0 - LSB

0	0	1	0	0	0	0	0
---	---	---	---	---	---	---	---

+--- allocate slot 0 for page 0
 +--- allocate slot 0 for page 1
 +--- allocate slot 2 for page 2
 +--- allocate slot 0 for page 3

The physical memory is always allocated to the same memory page in the CPU address space. It is not possible to allocate it to different page like page 3 of slot 3 to page 0 of CPU memory space.

- o Minimum system must have four slots, one for the main ROM, one for Sub ROM and two for external cartridge slot.
- o Main MSX2 BASIC ROM must be placed in primary slot 0 or the expanded slot 0-0. However application software should not assume that this ROM is in 0 or 0-0 because MSX2 cartridge for MSX1 will place the MSX2 BASIC ROM in a different slot. (Please see for notes for ISVs for more details.)
- o MSX2 SUB ROM can be placed in any slot. (always in page 0)
- o Shadow RAM in page 0 and 1 must be in same slot in order to support the MSX RAM DISK facility.

NOTE

The meaning of "slot" does not imply that it must have a connector for cartridge, however, the slot for the cartridge must have a connector, of course.

MSX-2 I/O ADDRESS MAP

NOTE

Address areas whose name has # symbol are not defined in MSX 1 specification. That is, those areas may be an image of previous devices so that the address decoding logic can be simplified. However, these area can be used for additional devices if the system fully decodes the address. But those devices should be managed between MSX machines to prevent possible address collision.

=====	
Undefined	

00-3F	
=====	
Switched I/O ports	

40	Enable / disable switch
41-4F	Switched I/O ports
=====	
Reserved	

50-7D	
=====	
MSX2 Key Cartridge	

7E-7F	

=====

RS-232C SUPPORT

80	8251 DATA
81	8251 STATUS/COMMAND
82	Status read/ interrupt mask
83	Not defined
84	8253
85	8253
86	8253
87	8253

=====

V D P (9938) for MSX-1 adapter

88-8B

NOTE

These addresses are for the adapter that include 9938 video chip and provide MSX-2 features for MSX-1 system. To keep the software compatibility between real MSX-2 system and MSX-1 system with MSX-2 adapter, which has video chip in above address, all MSX-2 software has to access video chip through the video chip address stored in ROM address 6 and 7.

=====

Modem

8C-8D	Usage is not specified
	Accessed through extended TELECOM BIOS call.

=====

Reserved

8E-8F

=====

Printer port

90 (w) bit 0 : strobe (r) bit 1 : status
91 print data (w) (r/w if bi-directional)
93 bi-directional control (option)

=====

Reserved #

92-97

=====

V D P (9938)

98-9B

=====

Reserved #

9C-9F

=====

Sound generator (AY-3-8910)

A0 Address latch
A1 Data write
A2 Data read
A3

=====

Reserved #

A4-A7

=====

Parallel Port (8255)

A8 PORT A
A9 PORT B
AA PORT C
AB MODE SET

=====

MSX-ENGINE #
(For the systems without MSX-ENGINE, these
areas may be an image of 8255)

AC-AF

=====

EXTERNAL MEMORY (SONY) (8255)

B0 PORT A ADDRESS A0-A7
B1 PORT B ADDRESS A8-A10, A13-A15, CONTROL, R/W
B2 PORT C ADDRESS A11-A12, D0-D7
B3 MODE SET

=====

CALENDAR CLOCK (RP-5C01 compatible)

B4 ADDRESS LATCH
B5 DATA

=====

Reserved

B6-B7

=====

LIGHT PEN CONTROL (same as SANYO)

B8 Read / Write
B9 Read / Write
BA Read / Write
BB Write only

=====

VHD CONTROL (JVC) (8255)

BC PORT A
BD PORT B
BE PORT C
BF MODE SET

=====

MSX Audio

C0-C1

=====

2nd MSX Audio (Option)

C2-C3

=====	
Reserved	

C4-C7	
=====	
MSX Interface	

C8-CF	
=====	
Floppy Disk Controller	

D0-D7	

NOTE

Above addresses are reserved for Floppy Disk Controller, however, it is not allowed to assign these addresses to specific hardware because the MSX disk system is designed to have multiple floppy disk controllers. So in a the system that uses these addresses for floppy disk controllers, they must be disabled and enabled only when accessed to prevent the bus collision with any other controller that uses above address. So we recommend putting floppy disk controllers in the memory address space.

=====	
Kanji Rom (same with TOSHIBA)	

D8	Kanji ROM
	b5-b0 Lower address (Write only)
D9	Kanji ROM
	b5-b0 Upper address (Write)
	b7-b0 Data (Read)

DA-DB	Reserved for future extension for KANJI.
=====	
24 dot Kanji ROM	

DC	Status (read)
	Lower Kanji code (write)
DD	Font data (read)
	Upper Kanji code (write)
=====	
Reserved	

DE-F4	

=====

System control

F5 Internal device enable (Write only)
Write 1 to enable internal device.

- b0 Kanji ROM
- b1 Reserved for Kanji
- b2 MSX-AUDIO
- b3 Super impose
- b4 MSX-INTERFACE
- b5 RS232C
- b6 Light pen
- b7 *Calendar clock

Since the calendar clock is a standard device for MSX-2, it is not necessary to have this bit, however, for the MSX-1, this bit is necessary.

NOTE

The purpose of these bits defined above is to prevent the collision of I/O devices which can be installed either as devices built into the system or through the cartridge slots. The built in devices can be disabled by above bits, and the system software checks if there is such a device installed through the cartridge slots and, if not, it turns on built in devices through above bits.

F6 Color bus I/O
Reserved to expand video function

F7 A/V control

- | | | | |
|----|--------------------------------------------|---|-------------------|
| b0 | Audio R | L | Mixing on (Write) |
| b1 | Audio L | L | Mixing on (Write) |
| b2 | Video input select | L | 21p RGB (Write) |
| b3 | Video input sense | L | No input (Read) |
| | Sync select | L | PC, H ext (Write) |
| b4 | AV CONTROL | L | TV (Write) |
| b5 | Ym CONTROL | L | TV (Write) |
| b6 | Complement of VDP Register 9 Bit 4 (write) | | |
| b7 | Complement of VDP register 9 Bit 5 (write) | | |

NOTE Complement of bit 4 and bit 5 of VDP Register 9 are placed in Bit 6 and 7 of I/O port 0F5H. The values of the bit 7 and 6 coorespond with the following display modes:-

- | B7 | B6 | Mode |
|----|----|-------------------------------------------------------------|
| 0 | 0 | Not used |
| 0 | 1 | TV |
| 1 | 0 | Computer/superimpose
(selected by TP bit of the MSX VDP) |
| 1 | 1 | computer |

=====

Reserved

```
=====
Memory Mapper
```

[illegible]

4.4 NOTES ON I/O ADDRESS ASSIGNMENTS

- o I/O address 40~FF are assigned for system usage. The empty areas are reserved for system use.

Although these addresses are defined here, software should not access those devices directly through the addresses listed above. Every access to the I/O must be done through the BIOS calls. This is to keep all software independent from hardware differences. Manufacturer may change some hardware from the standard MSX system but it is possible to maintain software compatibility by supporting the hardware differences within the BIOS, so that the difference can be transparent to the software.

Only exception is the access to VDP. Location 6 and 7 of MSX system ROM contains read and write address of VDP register. Any software that has to access VDP very quickly may do so directly through these addresses stored in ROM.

- o 00~3F are free addresses, however when different devices use the same address, they may not be accessed at the same time. Basically, special I/O devices not defined here should be placed in the memory space as memory mapped I/O. Refer to Appendix B.3
- % FDC may be placed in I/O space, but it must have the mechanism to disable it and ensure that it is enabled only when the system accesses the FDC. This makes it possible to have more than one FDC interface in the system.

4.5 8255 (PPI) BIT ASSIGNMENT

PORT	BIT	I/O	SIGNAL NAME	DESCRIPTION
A	0		CS0L	0000~3FFF address slot select signal
	1	O	CS0H	
	2	U	CS1L	4000~7FFF address slot select signal
	3	T	CS1H	
	4	P	CS2L	8000~BFFF address slot select signal
	5	U	CS2H	
	6	T	CS3L	C000~FFFF address slot select signal
	7		CS3H	
B	0	I		Keyboard return signal
	7	N P U T		
C	0		KB0	Keyboard scan signal
	1		KB1	
	2	O	KB2	
	3		KB3	
		U		
	4	T	CASON	Cassette control signal (L-ON)
	5	P	CASW	Cassette write signal
		U		
	6	T	CAPS	CAPS lamp signal ("L" --> ON)
	7		SOUND	Sound output by software

4.6 PSG BIT ASSIGNMENT

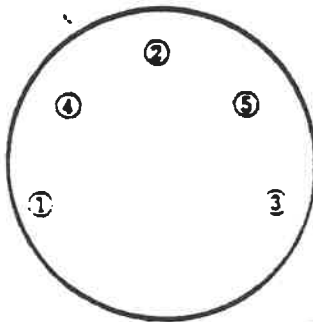
PORT	BIT	I/O	CONNECTOR PIN NO.		NOTE
A	0		J3-PIN 1	#1	FWD1
			J4-PIN 1 *	#2	FWD2
	1	I	J3-PIN 2	#1	BACK1
			J4-PIN 2 *	#2	BACK2
	2	N	J3-PIN 3	#1	LEFT1
			J4-PIN 3 *	#2	LEFT2
	3	P	J3-PIN 4	#1	RIGHT1
			J4-PIN 4 *	#2	RIGHT2
	4	U	J3-PIN 6	#1	TRGA1
			J4-PIN 6 *	#2	TRGA2
	5	T	J3-PIN 7	#1	TRGB1
			J4-PIN 7 *	#2	TRGB2
	6		KEY LAYOUT Select	#4	Japanese version only
	7		CSAR (CASSETTE TAPE READ)		
B	0		J3-PIN 6	#3	--
	1	O	J3-PIN 7	#3	"H" LEVEL
	2	U	J4-PIN 6 *	#3	
	3	T	J4-PIN 7 *	#3	--
	4	P	J3-PIN 8		
	5	U	J4-PIN 8 *		
	6	T	PORT A INPUT SELECT		Selects J3/J4
	7		KLAMP (KANA LAMP L- ON)		Japanese version only

- #1 Available when bit 6 of port B is low used by JOYSTICK1
 #2 Available when bit 6 of port B is HIGH used by JOYSTICK2
 #3 Turn to "H" level when use those pins as an input port.
 Tied an open collector buffer to the output. (Refer to Appendix C-1)
 #4 JIS layout - "H" level, syllable layout - "L" level

<Remark> PIN5 +5V
 PIN9 GND

PIN NAME	SPECIFICATION
1. Video output and composite video	DIN 5 PIN CONNECTOR 1 or RCA 2 PIN CONNECTOR
2. RF modulated signal	RCA 2 PIN CONNECTOR
CASSETTE	DIN 8 PIN CONNECTOR (DIN-45326)
I/O PORT	AMP 9 PIN CONNECTOR
PRINTER	UNPHENOL 14 PIN CONNECTOR
CARTRIDGE BUS	2.54 PACE, 50 PIN CONNECTOR
AUDIO	RCA 2 PIN CONNECTOR

1 DIN 5 PINS CONNECTOR SIGNAL PIN ASSIGNMENT

PIN NO.	NAME	PIN CONNECTION
1	+5V	
2	GND	
3	AUDIO	
4	MONITOR	
5	RF VIDEO	

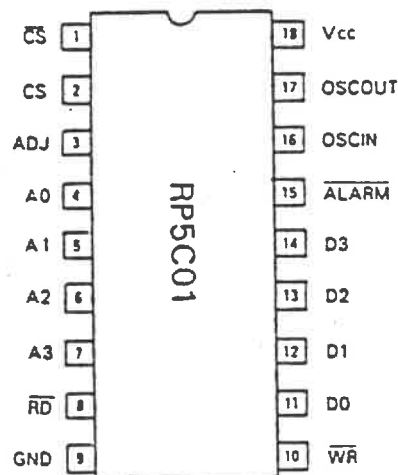
RICOH LSI NEWS

RP5C01 REAL TIME CLOCK

General

RP5C01 is the real time clock for micro computers, which is connected directly to the micro computer bus such as 8085A and Z80 and can set and read time in the same procedure as RAM. It has time and calendar counters, alarm function and 26×4 bits RAM, etc., allowing battery back up. Thus, it can be used as the non-volatile RAM.

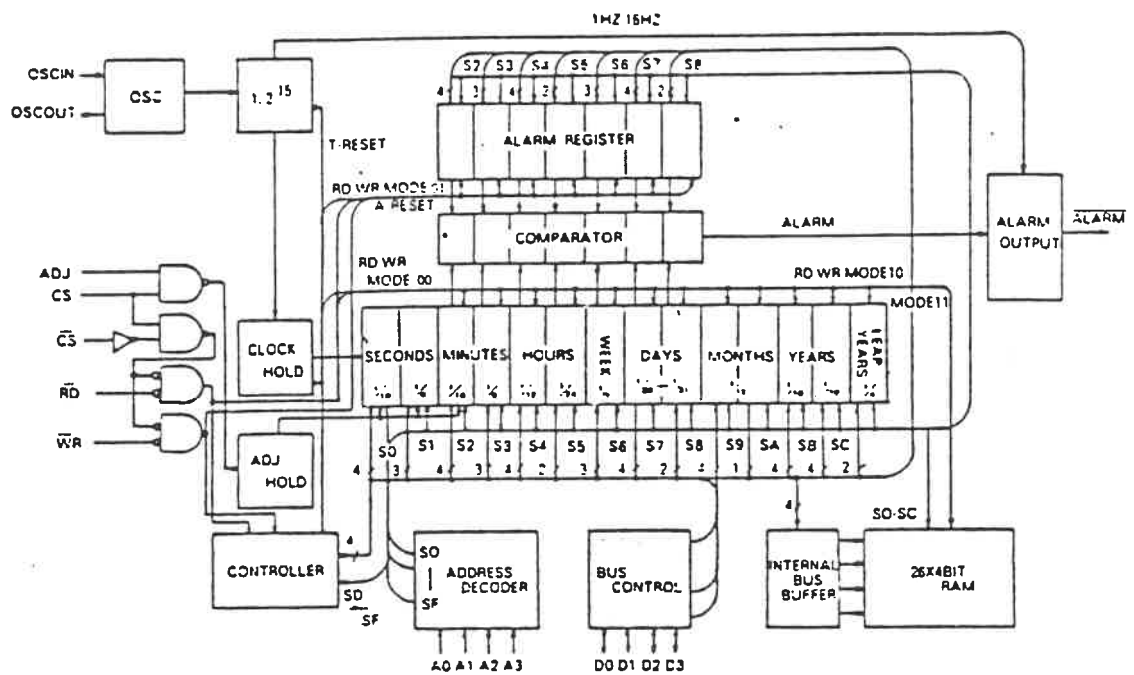
Terminal connection diagram



Features

- Directly connectable to CPU
- 4 bit dual duplex bus D₀ ~ D₃
- 4 bit address entry A₀ ~ A₃
- Time (second, minute, hour), calendar (date, day, month, leap year, 100 years) counters are included.
- Both 24 hour timer and 12 hour AM/PM timer are available
- All clock data are expressed in BCD code.
- ±30 sec. adjust function
- Battery back up is available.
- 26×4 bits RAM is included.
- Alarm signal or 16Hz or 1Hz timing pulse output is available.

Block diagram



Max. absolute rating

Symbol	Item	Condition	Rated value	Unit
V _{CC}	Power supply voltage	When GND terminal is reference	-0.3 ~ 7	V
V _I	Input voltage		-0.3 ~ 7	V
V _O	Output voltage		-0.3 ~ 7	V
P _O	Max. dissipation	T _a =25°C	700	mW
T _{opg}	Operation ambient temperature		0 ~ 70	°C
T _{stg}	Storage temperature		-40 ~ 125	°C

Recommended operational condition (T_a=0 ~ 70°C when not specified)

Symbol	Item	Rated value			Unit
		Min.	Standard	Max.	
V _{CC}	Power supply voltage	4.75	5	5.25	V
V _{DH}	Data saving voltage	2.2		5.25	V
f _{XT}	Cristal frequency		32.768		kHz

DC electrical characteristics (T_a=0 ~ 70°C, V_{CC}=5V±5%)

Symbol	Item	Measuring condition	Rated value			Unit
			Min.	Standard	Max.	
V _{IH}	"H" input voltage		2.0		V _{CC}	V
V _{IL}	"L" input voltage		-0.3		0.8	V
V _{OH}	"H" output voltage	I _{OH} =-400μA	2.4			V
V _{OL}	"L" output voltage	I _{OL} =2mA			0.4	V
I _c	Input current	V _I =0 ~ 5.25V			±10	μA
I _{oz}	Off output current				±10	μA
I _{CC1}	V _{CC} power supply current	f _{XT} =32.768kHz V _{CC} =2.2V			15	μA
I _{CC2}	V _{CC} power supply current	f _{XT} =32.768kHz V _{CC} =5.0V (Note 2)			250	μA

Note 1. Current incoming direction to IC is positive (no symbol).

Note 2. When connected to CPU (Read/Write Cycle 10μs).

AC electric characteristics (When not specified Ta=0 ~ 70°C, Vcc=5V±5%)

Symbol	Item	Measuring condition	value			Unit
			Min.	TYP	Max.	
tAC	Address RD/WR delay time		170			ns
tCC	RD/WR pulse width		400		10000	ns
tCA	Address valid time after RD/WR rising		10			ns
tRD	Data delay time after RD falling edge				340	ns
tRDH	Data hold time after RD rising edge		0			
tWDL	Data delay time after WR falling edge				40	ns
tWD	Data hold time after WR rising edge		20			

Standard values are as follows when Vcc=5V±10%.

AC electric characteristics (When not specified Ta=0 ~ 70°C, Vcc=5V±10%)

Symbol	Item	Measuring condition	Value			Unit
			Min.	TYP	Max.	
tAC	Address RD/WR delay time		170			ns
tCC	RD/WR pulse width		450		10000	ns
tCA	Address valid time after RD/WR rising		10			ns
tRD	Data delay time after RD falling edge				340	ns
tRDH	Data hold time after RD rising edge		0			ns
tWDL	Data delay time after WR falling edge				40	ns
tWD	Data hold time after WR rising edge		20			ns

RP5C01

REAL TIME CLOCK

Pin function

Pin name	Pin No.	Function
\overline{CS} , CS	1,2	The terminal for interfacing with external peripheral. Valid when CS-H and \overline{CH} =L CS is connected to power down detector. CS is connected to microcomputer.
ADJ	J	It can easily adjust second counter without CPU. When second is 0 ~ 29 with ADJ=H, second is set to 0. Minute is counted up and second is set to 0 for 30 ~ 59 seconds.
A ₀ ~ A ₃	4,5,6,7	ADDRESS pin. Connected to CPU address bus
\overline{RD}	8	I/O control input L when CPU-RP5C01
GND	9	OV
\overline{WR}	10	I/O control input L when CPU-RP5001
DO ~ D3	11,12,13	Duplex data bus. Connected to CPU data bus
	14	
\overline{ALARM}	15	Alarm signal and 16HzCK and 1HzCK pulse is outputted. Open drain output
OSCIN, OSCOU	16,17	Cristal oscillator connection terminal
V _{cc}	18	+5V power supply